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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

PP-4

Office Action Summary	Application No.	Applicant(s)	
	10/004,209	HUSE, CHARLES C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-43 are presented for examination.

Drawings

1. The drawings are objected to because FIG.11 "DBUS" is depicted with a left-hand arrow, when the examiner believes it should be a right-hand arrow. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: page 11 line 10 recites, "...device 100 is an...", but the examiner believes that it should read, "...device 100 in an...". Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: page 21 line 5 recites, "...the compare circuit 155...", but the examiner believes that it should read, "...the comparand circuit 150...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 36 recites the limitation "the index matches the second counter value" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 38 recites the limitation "the index matches the second counter value" in line 3 of the claim, and "the row of CAM cells that stores the first value. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 36 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: a reference to a preceding method and steps, where each of Claims 36 and 38 recites the step; "repeating the steps of claim 1". However, Claim 1 is not a method, and therefore does not recites steps. The examiner does not know which preceding method claim the applicant would like to reference, and so rejects the claims as being indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ichiriu et al., U.S. Patent No. 6597595.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per Claim 1:

Ichiriu et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a CAM array (see Abstract) that includes a plurality of rows of CAM cells (FIG.5 201) each coupled to match line (FIG.5 182); a priority encoder coupled to the match lines to generate an index (FIG.1 114); a counter (column 4 lines 27-30 and column 5 lines 32-38); and compare logic coupled to the counter and the priority encoder to compare the index and a counter value from the counter (FIG.25 and column 34 lines 57-63).

As per Claim 2:

Ichiriu et al. teaches the CAM device of claim 1, wherein the counter is an address counter (FIG.25 103 and column 4 lines 27-31).

As per Claim 3:

Ichiriu et al. teaches the CAM device of claim 1, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (column 5 lines 11-38).

As per Claim 4:

Ichiriu et al. teaches the CAM device of claim 3, wherein the address logic comprises a decoder (FIG.2 127).

As per Claim 5:

Ichiriu et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter and the address logic (FIG.2 125) to selectively output the count value (FIG.2 124) or an input address (FIG.2 141) for the address logic.

As per Claim 6:

Ichiriu et al. teaches the CAM device of claim 5, wherein the multiplexer is further coupled to the priority encoder (FIG.2 INDEX 174) to receive the index.

As per Claim 7:

Ichiriu et al. teaches the CAM device of claim 3, further comprising an instruction decoder (FIG.25 105) coupled to the address logic and adapted to decode instructions received by the CAM device (column 4 lines 54-64).

As per Claim 8:

Ichiriu et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or an input search key for the CAM array (FIG.16 540 and 531 and column 6 lines 1-13).

As per Claim 9:

Ichiriu et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or input data for the CAM array (FIG.16 540 and 531 and column 6 lines 1-13).

As per Claim 10:

Ichiriu et al. teaches the CAM device of claim 1, further comprising:

a write circuit coupled to the CAM array (FIG.25 161); and a comparand register coupled to the CAM array (FIG.25 115), the comparand register for storing a search key (column 3 lines 55-58).

As per Claim 11:

Ichiriu et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a counter (column 4 lines 27-30 and column 5 lines 32-38); and a CAM array having a plurality of rows of CAM cells (see Abstract) coupled to the counter (FIG.25 181) to receive a counter value as a search key for the CAM array (column 6 lines 1-13).

As per Claim 12:

Ichiriu et al. teaches the CAM device of claim 11, further comprising: a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells (FIG.25 114) and to generate an index (FIG.25 174); and compare logic coupled to the counter and the priority encoder to compare the index and the counter value (column 38 lines 1-7).

As per Claim 13:

Ichiriu et al. teaches the CAM device of claim 12, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.2 127).

As per Claim 14:

Ichiriu et al. teaches the CAM device of claim 13, further comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device (FIG.25 105).

As per Claim 15:

Ichiriu et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a counter (column 4 lines 27-30 and column 5 lines 32-38 and FIG.27 155); a CAM array (see Abstract and FIG.27 801) having a plurality of rows of CAM cells (FIG.27 801) coupled to the counter (FIG.127 803) to receive a counter value for storage in at least one of the rows of the CAM cells (FIG.27 155); and address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.27 807 and column 27 lines 11-39).

As per Claim 16:

Ichiriu et al. teaches the CAM device of claim 15, further comprising: a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells (FIG.25 114) and to generate an index (FIG.25 174); and compare logic (FIG.25 751) coupled to the counter (FIG.25 103 via 155) and the priority encoder to compare the index and the counter value (column 38 lines 1-8).

As per Claim 17:

Ichiriu et al. teaches the CAM device of claim 16, farther comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device (FIG.25 105).

As per Claim 18:

Ichiriu et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a CAM array (see Abstract) that includes a plurality of rows of CAM cells (FIG.5 201) each coupled to a match line (FIG.5 182); means for determining an index that indicates a location in the CAM array of one of one of the rows of CAM cells (FIG.25 114); means for generating an address of one of the rows of CAM cells in the CAM array (FIG.25 103); and means for determining that the address matches the index (FIG.25 715).

8. Claims 1-22, 25-36, and 39-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyatake et al., U.S. Patent No. 6539324.

As per Claim 1:

Miyatake et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a CAM array (FIG.1 1) that includes a plurality of rows of CAM cells (FIG.2 cell) each coupled to match line (FIG.2 Match0); a priority encoder coupled to the match lines to generate an index (FIG.1 3 and Search Address Bus); a counter (FIG.4 11 and column 5 lines 43-46); and compare logic coupled to the counter and the priority encoder to compare the index and a counter value from the counter (FIG.4 12 and column 5 lines 53-57).

As per Claim 2:

Miyatake et al. teaches the CAM device of claim 1, wherein the counter is an address counter (FIG.4 11 and column 5 lines 41-45).

As per Claim 3:

Miyatake et al. teaches the CAM device of claim 1, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.1 Address Bus to Address Decoder 4).

As per Claim 4:

Miyatake et al. teaches the CAM device of claim 3, wherein the address logic comprises a decoder (FIG.1 4).

As per Claim 5:

Miyatake et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter and the address logic (column 5 lines 53-57) to selectively output the count value (column 5 lines 40-45) or an input address (column 5 lines 19-33) for the address logic.

As per Claim 6:

Miyatake et al. teaches the CAM device of claim 5, wherein the multiplexer is further coupled to the priority encoder (FIG.4 Search Address Bus from Priority Encoder of FIG.1 3) to receive the index.

As per Claim 7:

Miyatake et al. teaches the CAM device of claim 3, further comprising an instruction decoder (FIG.4 10) coupled to the address logic and adapted to decode instructions received by the CAM device (FIG.4 CNTL).

As per Claim 8:

Miyatake et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or an input search key for the CAM array (column 5 lines 58-62).

As per Claim 9:

Miyatake et al. teaches the CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or input data for the CAM array (column 5 lines 58-62).

As per Claim 10:

Miyatake et al. teaches the CAM device of claim 1, further comprising: a write circuit coupled to the CAM array (FIG.1 5); and a comparand register coupled to the CAM array (FIG.1 6), the comparand register for storing a search key (FIG.4 9 Reference Data Bus/Data Bus).

As per Claim 11:

Miyatake et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a counter (FIG.4 11 and column 5 lines 43-46); and a CAM array (FIG.1 1) having a plurality of rows of CAM cells (FIG.2 cell) coupled to the counter (via Data Bus of FIG.1) to receive a counter value as a search key for the CAM array (column 5 lines 57-62).

As per Claim 12:

Miyatake et al. teaches the CAM device of claim 11, further comprising: a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells (FIG.1 3) and to generate an index (FIG.1 Search Address Bus); and compare logic coupled to the counter and the priority encoder to compare the index and the counter value (FIG.4 12).

As per Claim 13:

Miyatake et al. teaches the CAM device of claim 12, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.1 4).

As per Claim 14:

Miyatake et al. teaches the CAM device of claim 13, further comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device (FIG.4 10).

As per Claim 15:

Miyatake et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a counter (FIG.4 11 and column 5 lines 43-46); a CAM array (FIG.1 1) having a plurality of rows of CAM cells (FIG.2) coupled to the counter (FIG.1 Data Bus) to receive a counter value for storage in at least one of the rows of the CAM cells (column 5 lines 57-68); and address logic (FIG.1 4) coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.1 Address Bus).

As per Claim 16:

Miyatake et al. teaches the CAM device of claim 15, further comprising: a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells (FIG.1 3) and to generate an index (FIG.1 Search Address Bus); and compare logic (FIG.4 12) coupled to the counter (FIG.4 11) and the priority encoder to compare the index and the counter value (column 9 lines 29-30).

As per Claim 17:

Miyatake et al. teaches the CAM device of claim 16, farther comprising an instruction decoder coupled to the address logic (FIG.4 10) and adapted to decode instructions received by the CAM device (FIG.4 CNTL).

As per Claim 18:

Miyatake et al. teaches a content addressable memory (CAM) device (see Abstract), comprising: a CAM array (FIG.2) that includes a plurality of rows of CAM cells (FIG.1 1) each coupled to a match line (FIG.2 Match0); means for determining an index that indicates a location in the CAM array of one of one of the rows of CAM cells (FIG.1 2, 3); means for generating an address of one of the rows of CAM cells in the CAM array (FIG.1 3); and means for determining that the address matches the index (FIG.4 12).

As per Claim 19:

Miyatake et al. teaches a test system, comprising: a tester (FIG.1 7) that generates test signals (column 5 lines 19-33), and a content addressable memory (CAM) device (FIG.1 1,2,3,4,5,6) coupled to the tester to receive the test signals,

wherein the CAM device comprises a CAM array (FIG.1 1) that includes a plurality of rows of CAM cells (FIG.2) each coupled to a match line (FIG.2 Match0); a priority encoder coupled to the match lines (FIG.1 3) to generate an index (FIG.1 Search Address Bus); a counter (FIG.4 11); and a compare logic coupled to the counter and the priority encoder (FIG.4 12) to compare the index and a counter value from the counter (column 5 lines 34-61).

As per Claim 20:

Miyatake et al. teaches the test system of claim 19, wherein the compare logic has an output coupled to the tester to provide an indication of the comparison between the index and the counter value (FIG.4 13).

As per Claim 21:

Miyatake et al. teaches the test system of claim 20, wherein the CAM device further comprises address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.1 4).

As per Claim 22:

Miyatake et al. teaches the test system of claim 21, wherein the CAM device further comprises an instruction decoder coupled to the address logic (FIG.4 10), and wherein the test signals include instructions for the CAM device, and where the instruction decoder is adapted to decode the instructions transmitted to the CAM device.

As per Claim 25:

Miyatake et al. teaches a test system (FIG.1), comprising: a tester (FIG.1 7) that generates test signals (column 5 lines 19-33), a counter that generates a counter value (FIG.4 11 and column 5 lines 34-46); and a compare logic coupled to the counter (FIG.4 12); and a content addressable memory (CAM) device (FIG.1 1,2,3,4,5,6) coupled to the tester to receive the test signals (Address Bus, Data Bus), wherein the CAM device comprises: a CAM array (FIG.1 1) that includes a plurality of rows of CAM cells (FIG.2) each coupled to a match line (FIG.2 Match0); and a priority encoder coupled to the match lines (FIG.1 3) to generate an index (FIG.1 Search Address Bus), wherein the compare logic is coupled to the priority encoder (FIG.4 12) to compare the index and the counter value (column 5 lines 34-61).

As per Claim 26:

Miyatake et al. teaches the test system of claim 25, wherein the compare logic has an output coupled to the tester to provide an indication of the comparison between the index and the counter value (FIG.4 13).

As per Claim 27:

Miyatake et al. teaches the test system of claim 25, wherein the CAM device further comprises address logic coupled to the counter and the CAM array (FIG.1 4) to select at least one of the rows of CAM cells in the CAM array in response to the counter value (FIG.1 Address Bus and FIG.4 11).

As per Claim 28:

Miyatake et al. teaches the test system of claim 25, wherein the CAM device further comprises an instruction decoder coupled to the address logic (FIG.4 10), and

wherein the test signals include instructions for the CAM device (column 5 lines 19-33), and where the instruction decoder is adapted to decode the instructions transmitted to the CAM device (column 5 lines 19-33).

As per Claim 29:

Miyatake et al. teaches a method for operating a content addressable memory (CAM) device (column 9, line 15), comprising; systematically identifying locations in a CAM array of the CAM device that store data that match search keys; and synchronizing a counter within the CAM device with the identifying such that the identifications of the locations match counter values of the counter when the CAM device is operating properly (column 9 lines 20-36).

As per Claim 30:

Miyatake et al. teaches the method of claim 29, wherein the identifying comprises: comparing the search keys with the date stored in the CAM array (column 9 lines 40-43); and generating indices of the CAM array for the locations that store data that matches the search keys (column 10 lines 4-7).

As per Claim 31:

Miyatake et al. teaches the method of claim 29, further comprising comparing the indices with the counter values (column 9 lines 29-30).

As per Claim 32:

Miyatake et al. teaches a method for operating a content addressable memory (CAM) device (column 9, line 15), comprising: comparing a search key with data stored in a plurality of rows of CAM cells (column 9 lines 24-28); generating an index of a

location in the plurality of rows of CAM cells that indicates a match with the search key (column 10 lines 4-7); and comparing the index with a first counter value from a counter (column 9 lines 29-30).

As per Claim 33:

Miyatake et al. teaches the method of claim 32, wherein the data is the same for each of the rows of CAM cells (column 9 lines 17-19).

As per Claim 34:

Miyatake et al. teaches the method of claim 33, further comprising: masking CAM cells in a first of the rows of CAM cells corresponding to the first counter value; and identifying whether the index matches the first counter value (column 1 lines 27-36).

As per Claim 35:

Miyatake et al. teaches the method of claim 34, further comprising: unmasking the first row of CAM cells; and incrementing the counter to a second count value (column 1 lines 27-36).

As per Claim 36:

Miyatake et al. teaches the method of claim 35, further comprising: masking CAM cells in a second row of the CAM cells correspond to the second counter value; repeating the steps of claim 1; and identifying whether the index matches the second counter value (column 1 lines 27-36). Since "claim 1" does not contain steps, and since this claim is indefinite (see 112 rejections), the examiner believes that the rejection of this claim is based on the rejection above for Claim 35.

As per Claim 39:

Miyatake et al. teaches the method of claim 32, further comprising writing, prior to the first comparing step, a unique value to each of the rows of CAM cells such that a first row of the CAM cells having an address corresponding to the first counter value stores the first counter value, and a second row of the CAM cells having an address corresponding to a second counter value stores a second counter value (column 6 lines 14-29).

As per Claim 40:

Miyatake et al. teaches the method of claim 39, wherein the search key is the first count value (column 6 lines 30-46).

As per Claim 41:

Miyatake et al. teaches the method of claim 40, further comprising incrementing the counter to the second counter value (column 6 lines 30-46).

As per Claim 42:

Miyatake et al. teaches the method of claim 41, further comprising: comparing the second counter value with the data stored in the rows of CAM cells; generating another index of another location in the plurality of rows of CAM cells that stores the second counter value; and comparing the another index with the second counter value (column 6 lines 14-46).

As per Claim 43:

Miyatake et al. teaches a method (column 9, line 15) which would be adapted to a computer-readable medium having stored thereon sequence of instructions, systematically identifying locations in a CAM array of the CAM device that store data

that match search keys; and synchronizing a counter within the CAM device with the identifying such that the identifications of the locations match counter values of the counter when the CAM device is operating properly (column 9 lines 20-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 24, 37 and 38 are rejected under 35 U.S.C. 103(a) as being obvious over Ichiriu et al., U.S. Patent No. 6597595.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Claims 24, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyatake et al., U.S. Patent No. 6539324 as applied to Claims 19 and 33, and further in view of Ichiriu et al., U.S. Patent No. 6597595.

As per Claim 24:

Miyatake et al. teaches the test system of claim 19, but fails to teach; wherein the tester comprises a processor. In analogous art, for example, Ichiriu et al., in FIG.20 650, this feature is taught. And Ichiriu et al., in column 1 lines 50-68 describes various advantages of the invention, one being the ability to automatically invalidate data in the array during operation. One with ordinary skill in the art at the time of the invention, motivated as such by Ichiriu et al., would combine the art and so the claim is rejected.

As per Claim 37:

Miyatake et al. teaches the method of claim 33, but fails to teach: identifying whether the index matches the first counter value; invalidating the row of CAM cells that stores the first value; and incrementing the counter to a second counter value. However, in the analogous art of Ichiriu et al., this feature of invalidation is performed in reference to FIG.14. And Ichiriu et al., in column 1 lines 50-68 describes various advantages of the invention, one being the ability to automatically invalidate data in the array during operation. One with ordinary skill in the art at the time of the invention, motivated as such by Ichiriu et al., would combine the art and so the claim is rejected.

As per Claim 38:

Ichiriu et al. teaches the method of claim 37, further comprising: repeating the steps of claim 1; identifying whether the index matches the second counter value; and invalidating the row of CAM cells that stores the first value. Since "claim 1" does not contain steps, and since this claim is indefinite (see 112 rejections), the examiner believes that the rejection of this claim is based upon the above rejection of Claim 37.

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyatake et al., U.S. Patent No. 6539324 as applied to claim 19 above, and further in view of Agrawal, U.S. Patent No. 6341092. Miyatake et al. teaches the test system of claim 19, but fails to teach; wherein the tester comprises automated test equipment (ATE). In analogous art, for example Ichiriu et al., in column 1 lines 18-21, this feature is taught. And Agrawal in column 2 lines 40-43, describes the advantage of the invention, being the ability to test a CAM without addition of a large number of I/O pins. One with

ordinary skill in the art at the time of the invention, motivated as such by Agrawal, would combine the art, and so the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Albert DeCady
Primary Examiner